Claim Listing

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A computer implemented method comprising:

~~issuing~~ receiving a plurality of ~~operational~~ descriptors ~~to~~ at a controller, wherein the ~~operational~~ descriptors are ~~issued~~ received in a first order and wherein each ~~operational~~ descriptor includes a command **[[,]]** and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command ~~, and a value to be written upon completion of the command; and~~

~~indicating the completion status of each command in a second order, wherein the second order is different from the first order~~ ;

executing the command; and

upon completion of a command included in a respective descriptor, writing a completion status value for the command to the memory address external to the respective descriptor.

2. (cancelled)

3. (currently amended) The computer implemented method of claim 1 wherein the memory address included in the ~~operational~~ descriptor is an absolute address.

4. (currently amended) The computer implemented method of claim 1 wherein the memory address included in the ~~operational~~ descriptor is an offset from a base memory address.

5. (cancelled).

6. (original) The computer implemented method of claim 1 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

7. (original) The computer implemented method of claim 6 wherein the commands are grouped into categories depending on their execution times.

8. (original) The computer implemented method of claim 6 wherein the commands are grouped into categories depending on which of a plurality of resources executes them.

9. (original) The computer implemented method of claim 6 wherein each block of memory comprises a plurality of memory locations.

10. (original) The computer implemented method of claim 6 wherein each block of memory comprises a single memory location.

11. (original) The computer implemented method of claim 1 wherein the value to be written indicates the command's original location.

12. (currently amended) An article of manufacture comprising:

a machine-readable medium having instructions stored thereon to:

~~issue~~ receive a plurality of ~~operational~~ descriptors ~~to~~ at a controller, wherein the ~~operational~~ descriptors are ~~issued~~ received in a first order and wherein each ~~operational~~ descriptor includes a command **[[** , **]]** and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command ~~, and a value to be written upon completion of the command; and~~

~~indicate the completion status of each command in a second order, wherein the second order is different from the first order~~ ;

execute the command; and

upon completion of a command included in a respective descriptor, write a completion status value for the command to the memory address external to the respective descriptor.

13. (cancelled)

14. (currently amended) The article of manufacture of claim 12 wherein the memory address included in the ~~operational~~ descriptor is an absolute address.

15. (currently amended) The article of manufacture of claim 12 wherein the memory address included in the ~~operational~~ descriptor is an offset from a base memory address.

16. (previously presented) The article of manufacture of claim 12 wherein the value to be written indicates the command's original location.

17. (original) The article of manufacture of claim 12 wherein each command is stored in a first memory location, and the completion status of each command is written to a second memory location different from the first memory location.

18. (original) The article of manufacture of claim 12 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

19. (original) The article of manufacture of claim 18 wherein the commands are grouped into categories depending on their execution times.

20. (original) The article of manufacture of claim 18 wherein the commands are grouped into categories depending on which of a plurality of resources executes them.

21. (original) The article of manufacture of claim 18 wherein each block of memory comprises a plurality of memory locations.

22. (original) The article of manufacture of claim 18 wherein each block of memory comprises a single memory address.

23. (currently amended) An apparatus comprising:

a controller to accept a plurality of ~~operational~~ descriptors ~~to a controller~~, wherein the ~~operational~~ descriptors are ~~issued~~ received in a first order and wherein each ~~operational~~ descriptor includes a command **[[,]]** and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command ~~, and a value to be written upon completion of the command; and~~

executing the command; and

upon completion of a command included in a respective descriptor, writing a completion status for value the command to the memory address external to the respective descriptor~~.~~

~~wherein a completion status of each command is indicated in a second order, wherein the second order is different from the first order~~.

24. (cancelled)

25. (original) The apparatus of claim 23 wherein the commands are grouped into categories, and wherein the completion status of commands in each category are written to different blocks of memory locations.

26. (original) The apparatus of claim 25 wherein each block of memory locations comprises a plurality of memory locations.

27. (original) The apparatus of claim 25 wherein each block of memory locations comprises a single memory location.

28. (currently amended) A system comprising

a controller to accept a plurality of ~~operational~~ descriptors ~~to a controller~~, wherein the ~~operational~~ descriptors are ~~issued~~ received in a first order and wherein each ~~operational~~ descriptor includes a command **[[,]]** and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command ~~, and a value to be written upon completion of the command~~;;

a plurality of computational units, wherein the units execute commands from the respective ~~operational~~ descriptors; and

a memory providing the memory locations,

wherein upon completion of a command included in a respective descriptor, the controller writes a respective completion status value for the command to the memory address external to the respective descriptor~~.~~

~~a completion status of each command is indicated in a second order, wherein the second order is different from the first order~~.

29. (cancelled) .

30. (original) The system of claim 28 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

31. (original) The system of claim 30 wherein each block of memory locations comprises a plurality of memory locations.

32. (original) The system of claim 30 wherein each block of memory locations comprises a single memory location.

33. (currently amended) A computer implemented method comprising:

issuing a plurality of ~~operational~~ descriptors to a controller, each operation descriptor comprising a command; and

initiating executing the commands in a first order; and

indicating a completion status of each command, as each command completes, in the order that it completes, which is different from the first order.

34. (currently amended) The computer implemented method of claim 33 wherein each ~~operational~~ descriptor further comprises a memory address identifying a memory location to which the completion status for its respective command will be written, and a

value representing the completion status to be written upon completion of its respective command.

35. (new). The computer implemented method of claim 1

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms.

36. (new) The computer implemented method of claim 1 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command of the descriptor.

37. (new) The computer implemented method of claim 1

wherein writing a second completion status to a memory address external to a second descriptor occurs prior to writing a first completion status to a memory external to a first descriptor; and

wherein execution of a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

38. (new). The article of manufacture of claim 12

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms.

39. (new) The article of manufacture of claim 12 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of a command of the descriptor.

40. (new) The article of manufacture of claim 12 wherein writing a second completion status to a memory address external to a second descriptor occurs prior to writing a first completion status to a memory address external to a first descriptor and wherein execution of a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

41. (new). The apparatus of claim 25

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms .

42. (new). The apparatus of claim 41 wherein the controller comprises the multiple encryption units.

43. (new). The apparatus of claim 42 wherein the multiple encryption units comprise at least one of: (1) an Advanced Encryption Standard (AES) encryption engine; and (2) a Data Encryption Standard (DES) engine.

44. (new) The apparatus of claim 25 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command.

45. (new) The apparatus of claim 25 wherein the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein the controller comprises logic to execute a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

46. (new). The apparatus of claim 30

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms.

47. (new) The apparatus of claim 30 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command of the descriptor.

48. (new) The apparatus of claim 30 wherein the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein the controller comprises logic to initiate execution of a command in the first descriptor before initiating execution of a command in the second descriptor.